AMENDMENTS TO THE SPECIFICATION

[0006] The 2N and N+1 redundancy models provide protection from failures and improve availability. However, problems remain with these models as they are typically implemented. The 2N model can be inefficient. That is, since completely redundant systems are used, utilization of resources may not be efficient. Models with ~~a redundant CPUs~~ a redundant CPU present difficulties in environments where they share a bus such as the N+1 model since only one device at a time may control the bus. Additionally, a switch-over following a CPU failure generally requires a power-down or reset of the remaining CPU before it can take over for the failed CPU. This interrupts service.

[0025] Importantly, while embodiments of the present invention will be described with reference to the Redundant System Slot specification and ~~CompactPCI~~ COMPACTPCI as described in the ~~CompactPCI~~ COMPACTPCI Redundant System Slot Specification PICMG 2.13 Draft 0.51 May 03, 2001 cited in an IDS, the method and apparatus described herein are equally applicable to other redundant systems and bus standards.

[0035] System master - A board within a ~~CompactPCI~~ COMPACTPCI system that provides arbitration, clock distribution, reset, interrupt, and enumeration functions to peripheral slots. In a non-redundant configuration, the system master represents a single point of failure. In a redundant configuration the signals necessary to provide system master functions are also connected to a redundant system master that becomes active in the event of a failure.

[0036] System slot - A location on a ~~CompactPCI~~ COMPACTPCI backplane in which a system master may be placed.

[0037] The Redundant System Slot (RSS) standard, as will be summarized below, is described in the ~~CompactPCI~~ COMPACTPCI Redundant System Slot Specification PICMG 2.13 Draft 0.51 May 03, 2001 cited in an IDS. Briefly, this standard describes a redundant system with characteristics similar to the N+1 redundancy model described above. Generally, the system includes a system slot board that is much like a motherboard in PC. This system slot board provides control functions like clock, bus arbitration etc. However, prior implementations of RSS systems allow only one system slot board at a time to provide these functions to a particular bus segment. Further details of the RSS system are described below.

[0039] Each system master 305 and 310 is connected with two bus segments 340 and 345. These bus segments 340 and 345 are typically ~~CompactPCI~~ COMPACTPCI busses but may be another bus architecture. The system masters 305 and 310 are each connected with the bus segments 340 and 345 via PCI-to-PCI bridges 320-335. The details of these bridges will be discussed below with reference to figure 7. Each bus segment 340 and 345 is also connected with a number of peripherals 350 and 355. These peripherals can be of any type compatible with the bus architecture used by the two bus segments 340 and 345.

[0047] **Figure 7** is a block diagram illustrating a Redundant System Slot (RSS) architecture upon which embodiments of the present invention may be implemented. In this system 700, two system master boards are shown 701 and 702. In this example, one system master 701 is acting as an active host while the other system master 702 is acting as a standby host. The two system masters 701 and 702 are connected with each other via an Ethernet link 735, two busses 740 and 750, and a host control line 745. The Ethernet

link 735 is used primarily for maintaining synchronization between the two system masters 701 and 702 during normal operations so that the standby host 702 is ready to takeover control of devices attached to the active host 701 in event of a failure. Of course, this link 735 may be of another type, such as a simple serial or parallel link. The two busses 740 and 750 are used to provide both system masters 701 and 702 with access to peripheral devices connected with these busses 740 and 750. In this example, a ~~CompactPCI~~ COMPACTPCI bus is indicated but other bus standards may be used as well. The host control line 745 is provided to allow for coordinated control of the two busses 740 and 750 between the two system masters 710 and 702. For example, this line 745 will be used to pass control signals used during startup and at the time of fail-over, such as requesting and sending maps of bus devices, indicating a system master's mode of operation, and sending failure notifications.

[0048] Each system master 701 and 702 contains a communications module 715, PCI-to-PCI bridges 720, clocks 730, and a Redundant Host Controller (RHC). The communication modules 715, connected with the Ethernet link 735, are used primarily for maintaining synchronization between the two system masters 701 and 702 during normal operations so that the standby host 702 is ready to takeover control of devices attached to the active host 701 in event of a failure. The PCI-to-PCI bridges 720, together with the two busses 740 and 750, are used to provide the system masters 701 and 702 with access to peripheral devices connected with these busses 740 and 750. In this example, a ~~CompactPCI~~ COMPACTPCI bus is indicated but other bus standards may be used as well. The functions of the clocks 730 are to provide required clock signals to the two busses 740 and 750. Finally, the Redundant Host Controller (RHC), together with the host control line 745, is used to provide bus arbitration on the two busses 740 and 750

and allow for coordinated control of the two busses 740 and 750 between the two system masters 701 and 702. For example, the RHC will generate, receive, and respond to control signals used during startup and at the time of fail-over such as requesting and sending maps of bus devices, indicating a system master's mode of operation, and sending failure notifications.

[0050] Also included in the RHC 800 are a P2P bridge control module 815, a bus arbiter and control module 825, a power and reset control module 830, a clock control module 835 and a host controller interface unit 820. The P2P (PCI-to-PCI) bridge control module ~~715~~ 720, together with the two busses 740 and 750 discussed above, are used to provide system masters with access 850 to peripheral devices connected with these busses 740 and 750. The bus arbiter and control module 825 is used to provide 860 bus arbitration on the two busses 740 and 750 and allow for coordinated control of the two busses 740 and 750 between system masters. The clock control module provides required clock signals 865 to the two busses 740 and 750. Finally, the HC interface unit 820 will generate, receive, and respond to control signals 855 used during startup and at the time of fail-over such as requesting and sending maps of bus devices, indicating a system master's mode of operation, and sending failure notifications.

[0054] The high available manager 940 provides an interface between the bridge and peripheral drivers 935 and the host controller drivers 945. Generally, the high availability manager monitors installed drivers for peripherals connected with the busses 970 to determine whether they are compatible with the host controller driver. In one embodiment of the present invention, this compatibility may be based on the ~~well-know~~ well-known High Availability (HA) requirements for ~~CompactPCI~~ COMPACTPCI

devices as described in the ~~CompactPCI~~ COMPACTPCI Redundant System Slot Specification PICMG 2.13 Draft 0.51 May 03, 2001 cited in an IDS.